App. Serial No.: 09/051,263
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IN THE CLAIMS

Please amend the claims as follows:

1. (currently amended) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said ~~central processing unit~~ microprocessing unit and to said IOP, and means for arbitrating access of said ~~central processing unit~~ microprocessing unit and said IOP to said global memory unit, wherein said microprocessing unit further comprises an arithmetic logic unit that is used for data operations and for branch address calculations.

2. (original) The microprocessor system of claim 1 in which said global memory unit comprises a plurality of global registers.

3. (currently amended) The microprocessor system of claim 1 wherein said ~~central processing unit~~ microprocessing unit includes an arithmetic logic unit and a push-down stack coupled to said arithmetic logic unit.

4. (original) The microprocessor system of claim 1 further including a memory interface unit coupled to said global memory unit, to said microprocessing unit, and to said IOP.

5. (original) The microprocessor system of claim 4 further including a means for arbitrating access of said memory interface unit and said microprocessing unit to said global memory unit.

6. (original) The microprocessor system of claim 5 additionally comprising a system memory and at least one input-output device coupled to said memory interface unit and wherein each storage location in said global memory unit holds a single address comprised of a first grouping of address bits coupled to address said system memory and a second grouping of address bits coupled to address said at least one input-output device.

7. (original) The microprocessor system of claim 5 additionally comprising a system memory, at least one input-output device and a system bus coupled to said memory interface unit, said system bus having a first grouping of address lines coupled to address said system memory and a second grouping of address lines coupled to address said at least one input-output device.

8. (currently amended) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said ~~central processing unit~~ microprocessing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals, wherein said microprocessing unit fetches multiple sequential instructions from memory in parallel, and said memory supplies said multiple sequential instructions to said microprocessing unit during a single memory cycle.

9. (original) The microprocessor system of claim 8 wherein said memory interface unit includes means for defining available time slots during which said system bus may be accessed, said available time slots being defined as being between accesses to said system bus by said IOP at said predetermined intervals.

10. (currently amended) The microprocessor system of ~~claim 8~~ claim 9 wherein said memory interface unit includes means for computing a bus access time required for one or more bus cycles involving said system bus, and for allocating one of said available time slots equal to or longer than said access time for execution of said one or more bus cycles.

11. (original) The microprocessor system of claim 10 wherein said one or more bus cycles are memory cycles.

12. (original) The microprocessor system of claim 11 in which the computation of said means for computing modifies the bus access time to provide sufficient time for input-output cycles.

13-26. (canceled)

27. (currently amended) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), and a memory interface unit selectively coupling said ~~central processing unit~~ microprocessing unit and said IOP to a system bus, said IOP including program counter means for providing system address information to said memory interface unit, wherein bus transaction requests are arbitrated and prioritized by said memory interface unit.

28. (original) The microprocessor system of claim 27 further including means, coupled to said IOP and to said system bus, for granting said IOP access to said system bus at predetermined intervals.

29. (original) The microprocessor system of claim 27 wherein said IOP includes latch means, coupled to said system bus, for latching data received from said system bus.

30. (original) The microprocessor system of claim 27 wherein said IOP includes a multiplexer controlled by said program counter means, an instruction latch, and a decode/execute module, said multiplexer coupled between said instruction latch and said decode/execute module.

31-44. (canceled)

45. (new) A microprocessor system, comprising:
a microprocessing unit (MPU);
an input-output processor (IOP);
a global memory unit coupled to said MPU and to said IOP;
a direct memory access controller (DMAC);
an interrupt controller (INTC);
a programmable memory interface (MIF);
an external CMOS oscillator, operating in conjunction with a clock multiplier;
a plurality of bit inputs; and
a plurality of bit outputs.

46. (new) The microprocessor system of claim 45, wherein:
a frequency of said oscillator is quadrupled internally to operate said MPU and said IOP.

47. (new) The microprocessor system of claim 45, wherein:
said microprocessor system utilizes a phase locked loop circuit.

48. (new) The microprocessor system of claim 45, wherein:
said MPU retrieves up to four instructions from memory for each instruction fetch or pre-fetch.

49. (new) The microprocessor system of claim 45, wherein:
said MPU fetches multiple sequential instructions from said global memory unit in parallel, and said global memory unit supplies said multiple sequential instructions to said MPU during a single memory cycle.

50. (new) The microprocessor system of claim 45, wherein:
said MPU further comprises an arithmetic logic unit (ALU) that is used for data operations and for branch address calculations.

51. (new) The microprocessor system of claim 45, wherein:
said MPU further comprises an arithmetic logic unit (ALU), and a first push down stack with a top item register and a next item register, connected to provide inputs to said ALU, an output of said ALU being connected to said top item register.

52. (new) The microprocessor system of claim 45, wherein:
said MPU comprises a zero-operand dual-stack architecture.

53. (new) The microprocessor system of claim 52, wherein:
said dual-stack architecture is cached on chip and automatically spills to and refills from external memory.

54. (new) The microprocessor system of claim 45, wherein:
said MPU comprises a plurality of global data registers and a plurality of local registers.

55. (new) The microprocessor system of claim 45, wherein:
said global memory unit is shared by said MPU, said IOP, and said MIF.

56. (new) The microprocessor system of claim 45, wherein:
said global memory unit is used for data storage and control communication with said DMAC and said IOP.

57. (new) The microprocessor system of claim 45, wherein:
said global memory unit is used by said IOP for transfer information, loop counts, and delay counts.

58. (new) The microprocessor system of claim 45, wherein:
said MIF is shared by said IOP, said MPU, said DMAC, said plurality of bit outputs, and said plurality of bit inputs.

59. (new) The microprocessor system of claim 45, wherein:
bus transaction requests are arbitrated and prioritized by said MIF.

60. (new) The microprocessor system of claim 45, wherein:
said INTC is shared by said plurality of bit inputs, said IOP, and said DMAC.

61. (new) The microprocessor system of claim 45, wherein:
said global memory unit comprises a plurality of global registers.

62. (new) The microprocessor system of claim 61, wherein:
said plurality of global registers are used for operand storage for said MPU, and for data storage for said IOP.

63. (new) A microprocessor system, comprising: a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said microprocessing unit and to said IOP, and means for arbitrating access of said microprocessing unit and said IOP to said global memory unit, wherein said microprocessing unit retrieves up to four instructions from memory for each instruction fetch or pre-fetch.

64. (new) A microprocessor system, comprising: a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said microprocessing unit and to said IOP, and means for arbitrating access of said microprocessing unit and said IOP to said global memory unit, wherein said microprocessing unit fetches multiple sequential instructions from said global memory unit in parallel, and said global memory unit supplies said multiple sequential instructions to said microprocessing unit during a single memory cycle.

65. (new) A microprocessor system, comprising: a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said microprocessing unit and to said IOP, and means for arbitrating access of said microprocessing unit and said IOP to said global memory unit, wherein said microprocessing unit comprises a zero-operand dual-stack architecture.

66. (new) The microprocessor system of claim 65, wherein said dual-stack architecture is cached on chip and automatically spills to and refills from external memory.

67. (new) A microprocessor system, comprising: a microprocessing unit, an input-output processor (IOP), a global memory unit coupled to said microprocessing unit and to said IOP, and means for arbitrating access of said microprocessing unit and said IOP to said global memory unit, wherein said global memory unit is used by said IOP for transfer information, loop counts, and delay counts.

68. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said microprocessing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals, wherein said microprocessing unit retrieves up to four instructions from memory for each instruction fetch or pre-fetch.

69. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said microprocessing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals, wherein said microprocessing unit further comprises an arithmetic logic unit that is used for data operations and for branch address calculations.

70. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said microprocessing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals, wherein said microprocessing unit comprises a zero-operand dual-stack architecture.

71. (new) The microprocessor system of claim 70, wherein: said dual-stack architecture is cached on chip and automatically spills to and refills from external memory.

72. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), a memory interface unit through which said microprocessing unit and said IOP are selectively coupled to a system bus, and means for granting said IOP access to said system bus at predetermined intervals, wherein bus transaction requests are arbitrated and prioritized by said memory interface unit.

73. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), and a memory interface unit selectively coupling said microprocessing unit and said IOP to a system bus, said IOP including program counter means for providing system address information to said memory interface unit, wherein said microprocessing unit retrieves up to four instructions from memory for each instruction fetch or pre-fetch.

74. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), and a memory interface unit selectively coupling said microprocessing unit and said IOP to a system bus, said IOP including program counter means for providing system address information to said memory interface unit, wherein said microprocessing unit further comprises an arithmetic logic unit that is used for data operations and for branch address calculations.

75. (new) A microprocessor system, comprising a microprocessing unit, an input-output processor (IOP), and a memory interface unit selectively coupling said microprocessing unit and said IOP to a system bus, said IOP including program counter means for providing system address information to said memory interface unit, wherein said microprocessing unit comprises a zero-operand dual-stack architecture.

76. (new) The microprocessor system of claim 75, wherein: said dual-stack architecture is cached on chip and automatically spills to and refills from external memory.